OpenPiton in Action

Princeton University

- PLEASE DOWNLOAD AND INSTALL Virtual Box
- PLEASE DOWNLOAD AND INSTALL Putty (Windows)

http://openpiton.org

OpenPiton

OpenPiton in Action

Princeton University

http://openpiton.org

Princeton Parallel Research Group

- Redesigning the Data Center of the Future
  - Chip Architecture
  - Operating Systems and Runtimes
  - Power and Cooling Optimization
- Biodegradable Computing (Materials)

- 12 PhD Students
- 3 Undergraduates

Winter 2018 Ski Trip

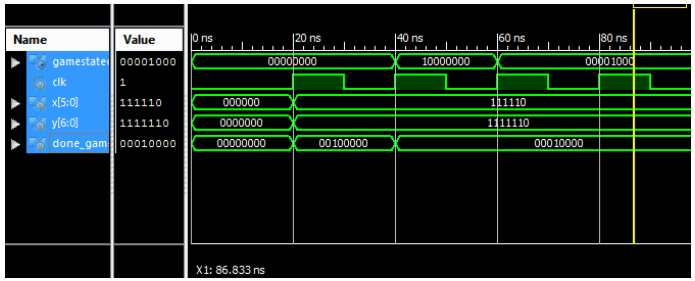
Support

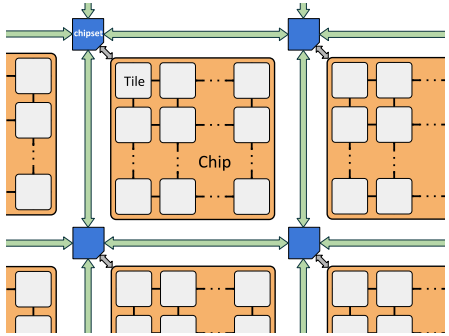
This work was partially supported by the NSF under Grants No. CCF-1217553, CCF-1453112, and CCF-1438980, AFOSR under Grant No. FA9550-14-1-0148, and DARPA under Grants No. N66001-14-1-4040 and HR0011-13-2-0005. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of our sponsors.

The world's first open source, general purpose, multithreaded manycore processor

- Open source (GPL core, BSD uncore) manycore
- Written in Verilog RTL
- Scales to ½ billion cores
- Configurable core, uncore
- Includes synthesis and back-end flow
- ASIC & FPGA verified
- ASIC power and energy fully characterized [HPCA 2018]
- Runs full stack multi-user Debian Linux
- Great for Architecture, Programming Language, Compilers, Operating Systems, Security, EDA research

GPL BSD



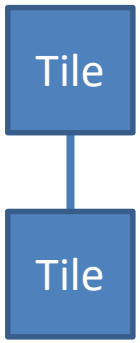


debian

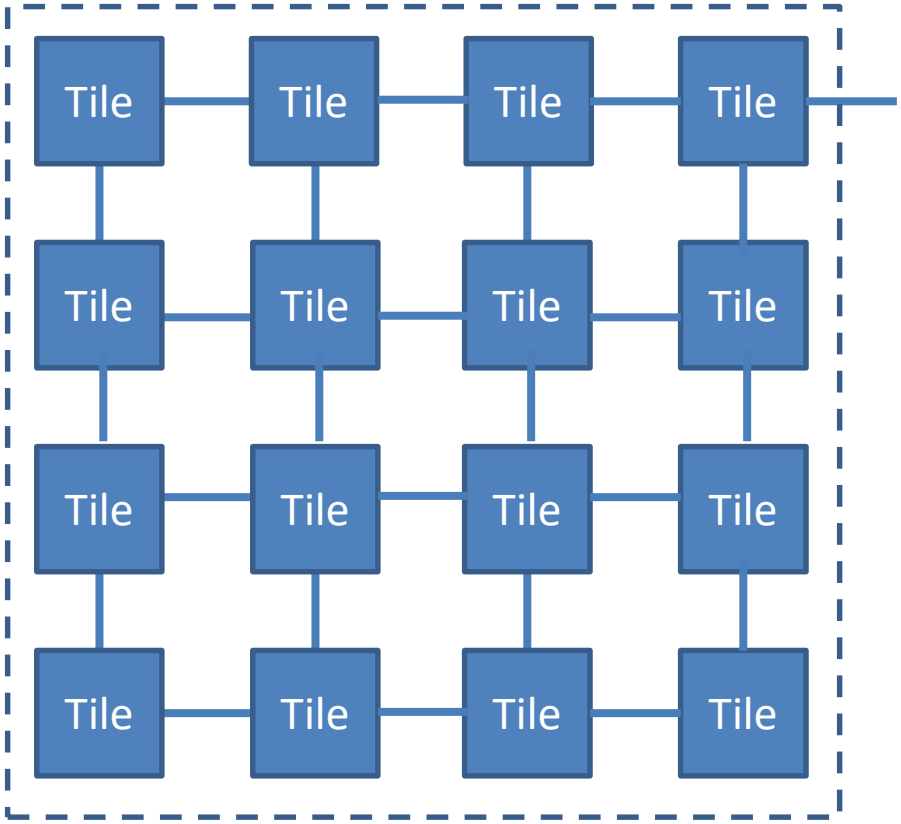
XILINX®

OpenPiton System Overview

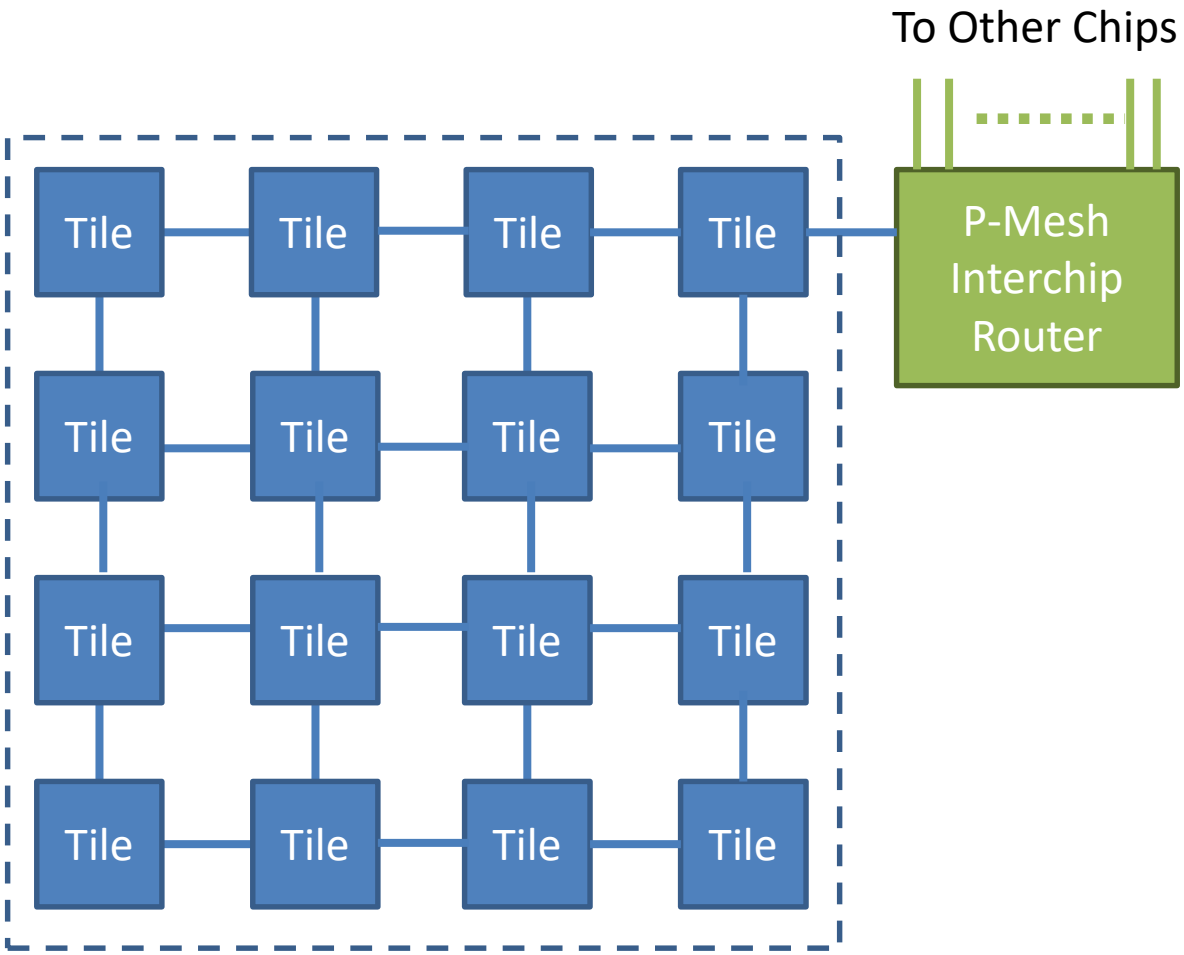
OpenPiton System Overview



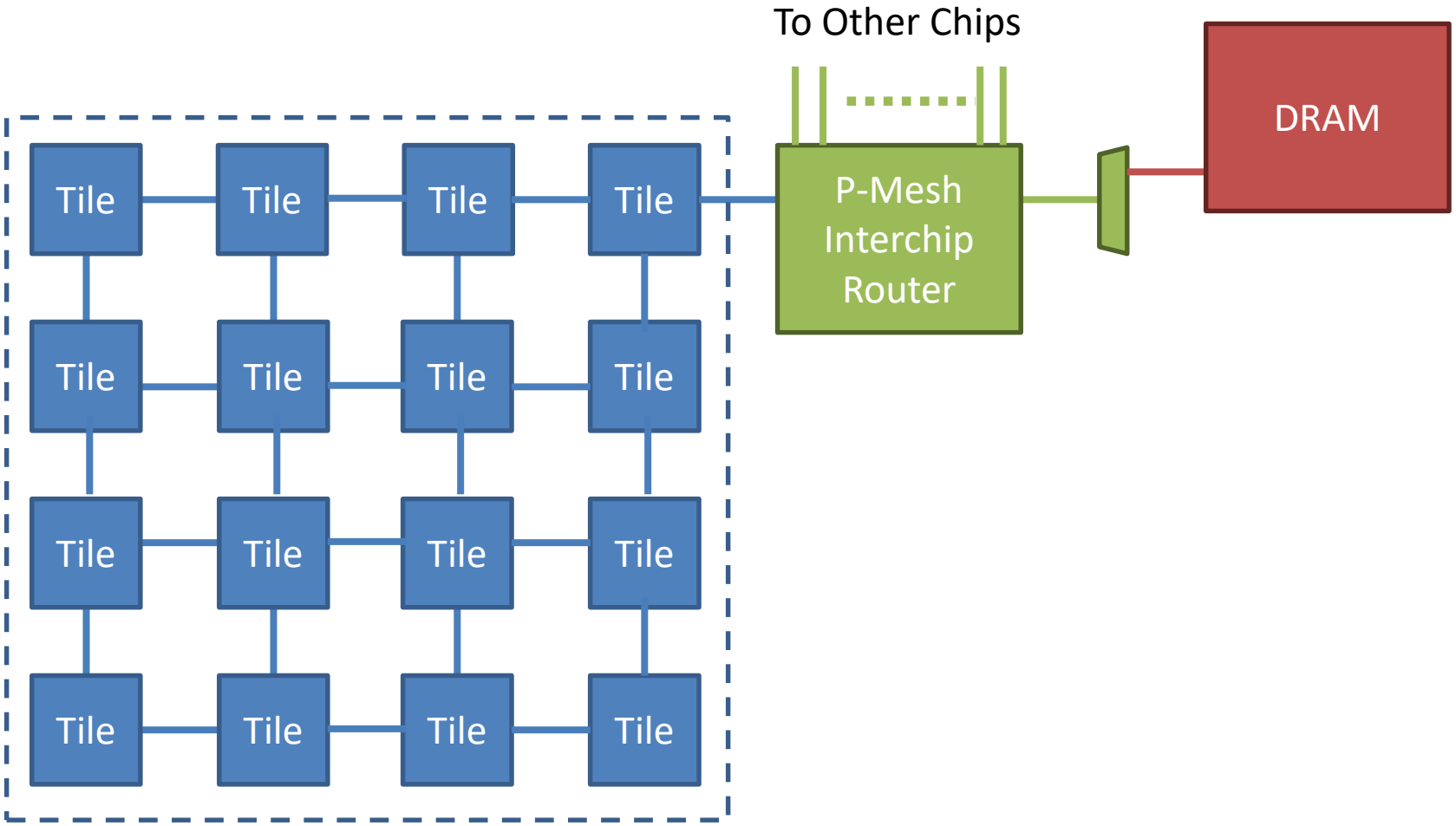
OpenPiton System Overview



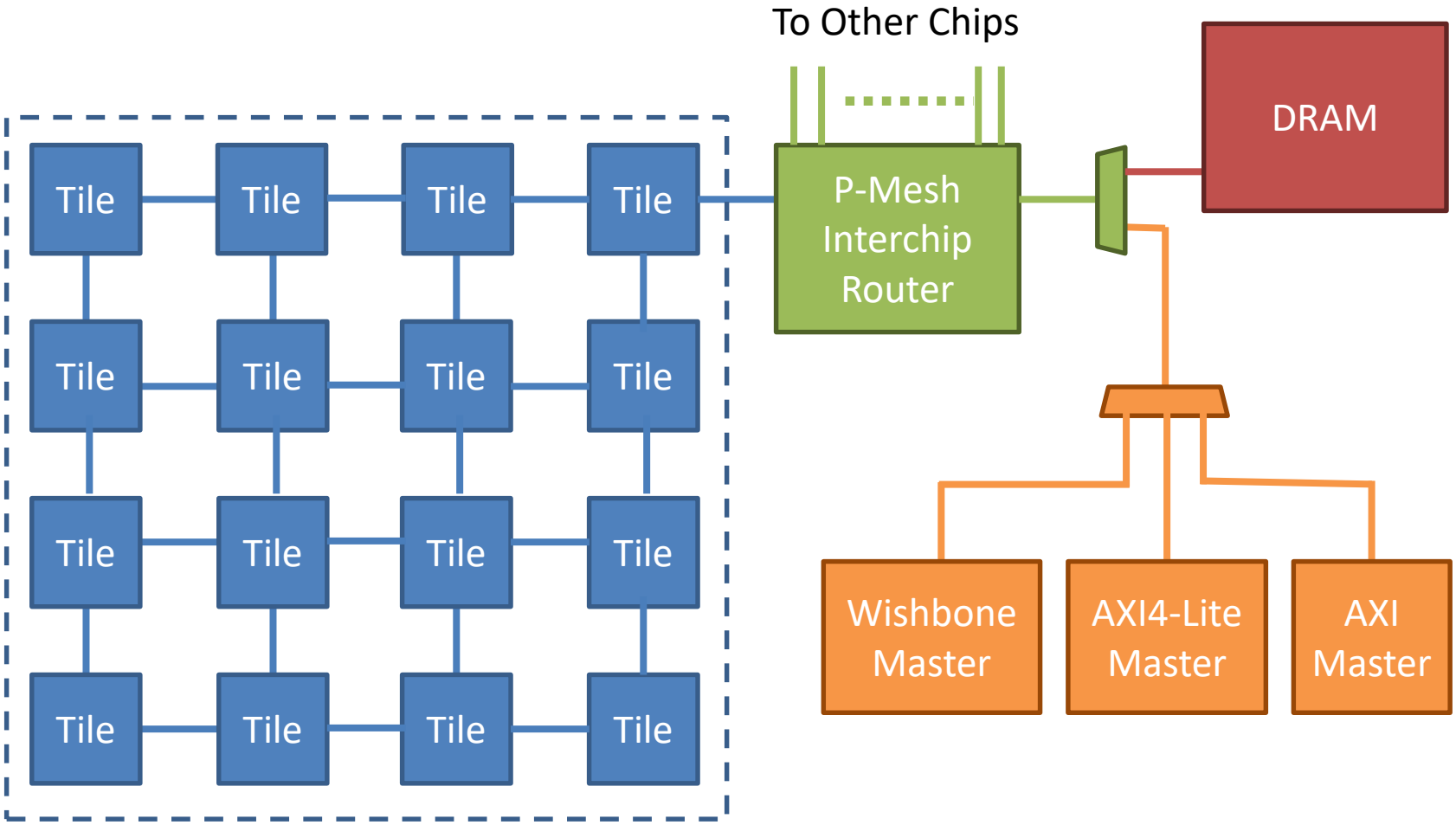
OpenPiton System Overview



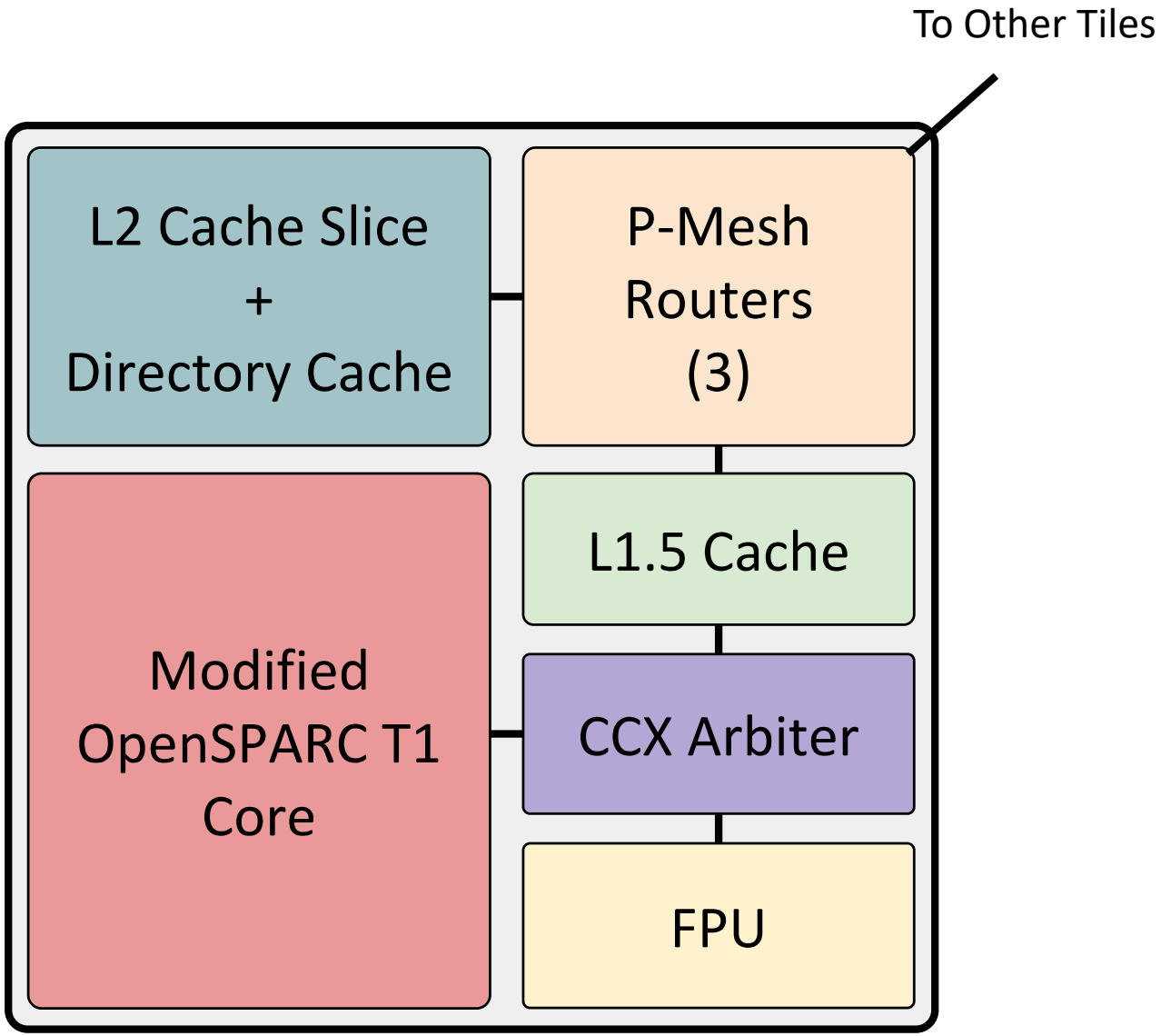
OpenPiton System Overview



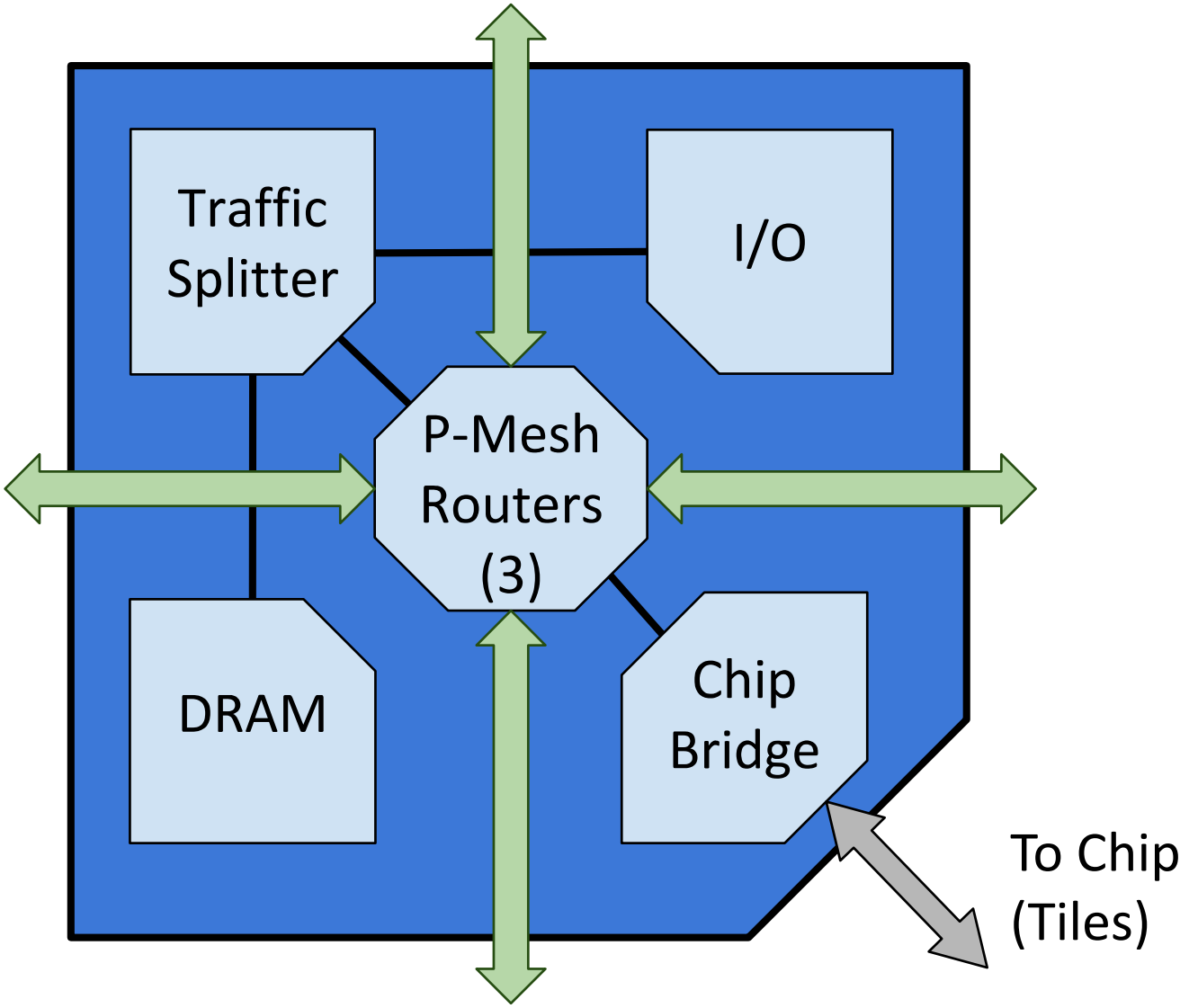
OpenPiton System Overview



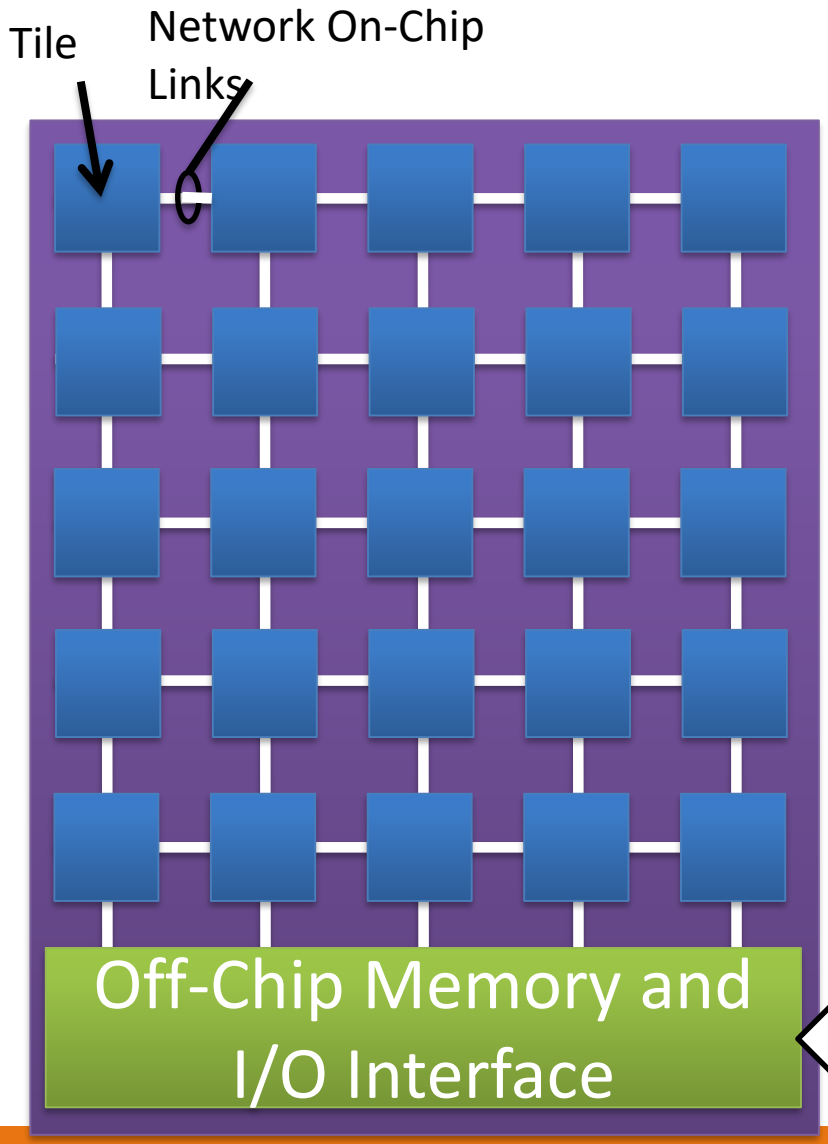
Tile Overview



Chipset Overview



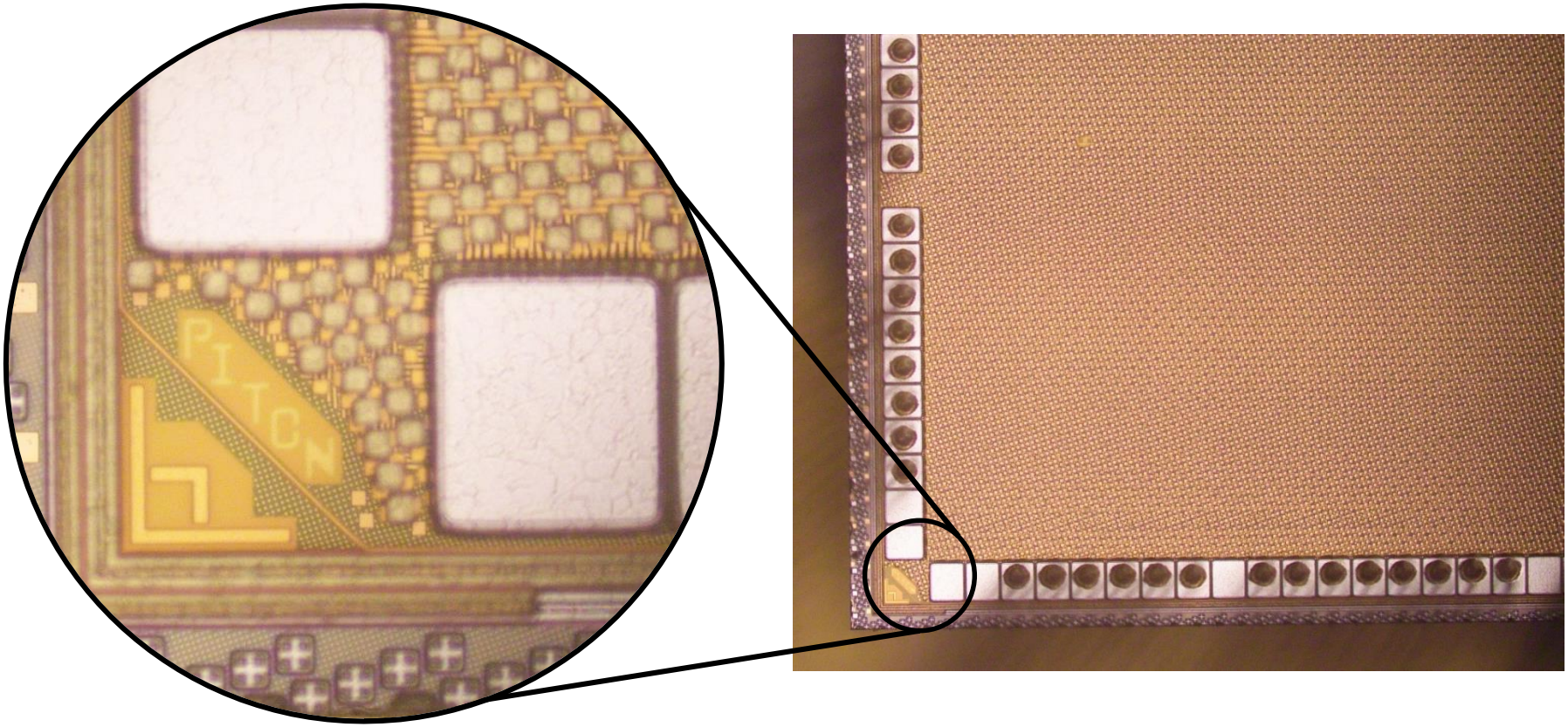
Piton Chip Block Diagram



- 25-core
  - 2 Threads per core
  - 64-bit Architecture
  - Modified OpenSPARC T1 Core
- 3 NoCs (P-Mesh)
  - 64-bit, 2D Mesh
  - Extend off-chip enabling multichip systems
- Directory-Based Cache System
  - 64KB L2 Cache per core (Shared)
  - 8KB L1.5 Data Cache
  - 8KB L1 Data Cache
  - 16KB L1 Instruction Cache
- IBM 32nm SOI Process
  - 6mm x 6mm
  - 460 Million Transistors
- Target: 1GHz Clock @ 900mV
- 208 Pin CQFP Package

Piton Layout

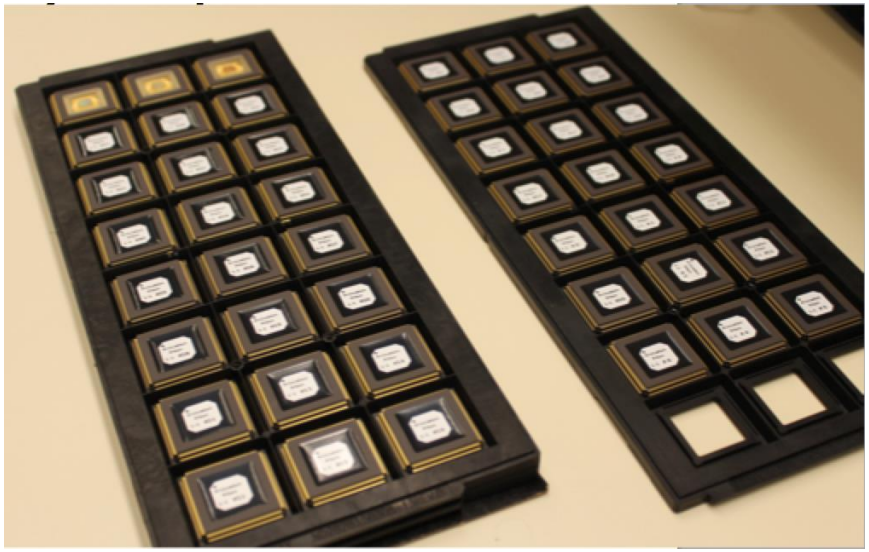
Piton Chip

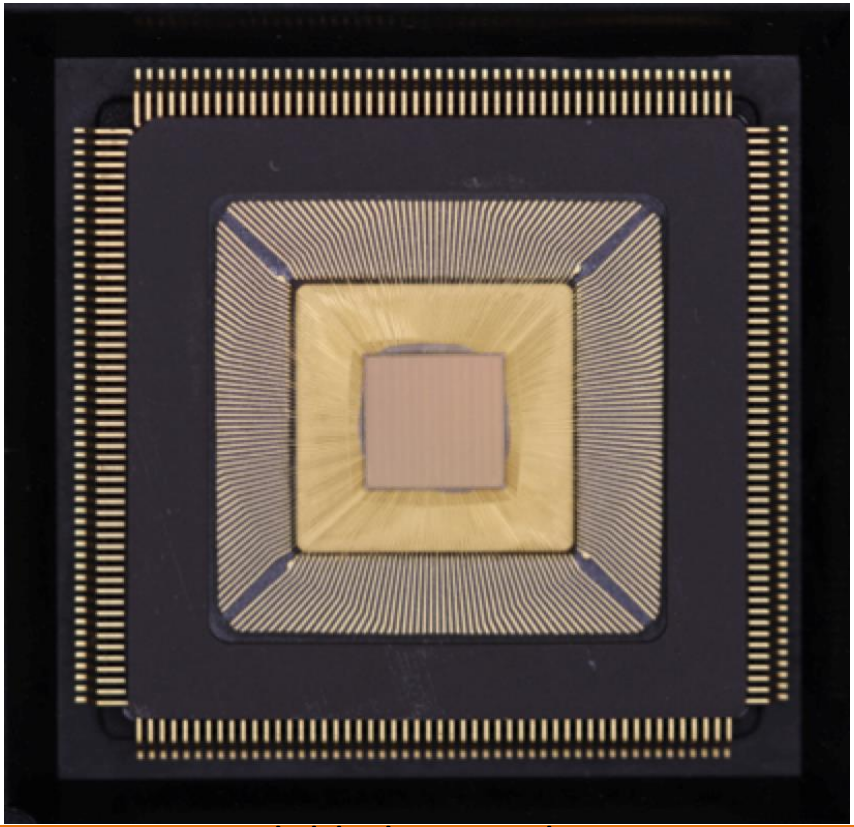


- Among largest chips ever built in academia
- Received silicon and has been tested working in lab

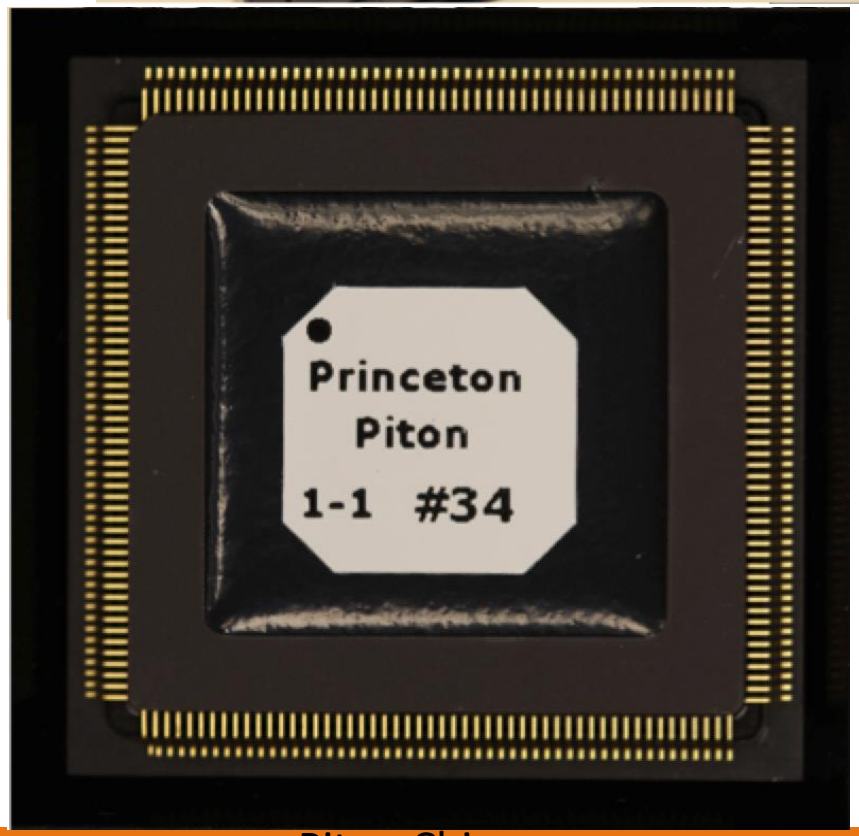
Piton Chip

- Piton Processor packaged in 208-pin Ceramic Quad Flat Pack (CQFP)
- Received ~100 die from IBM



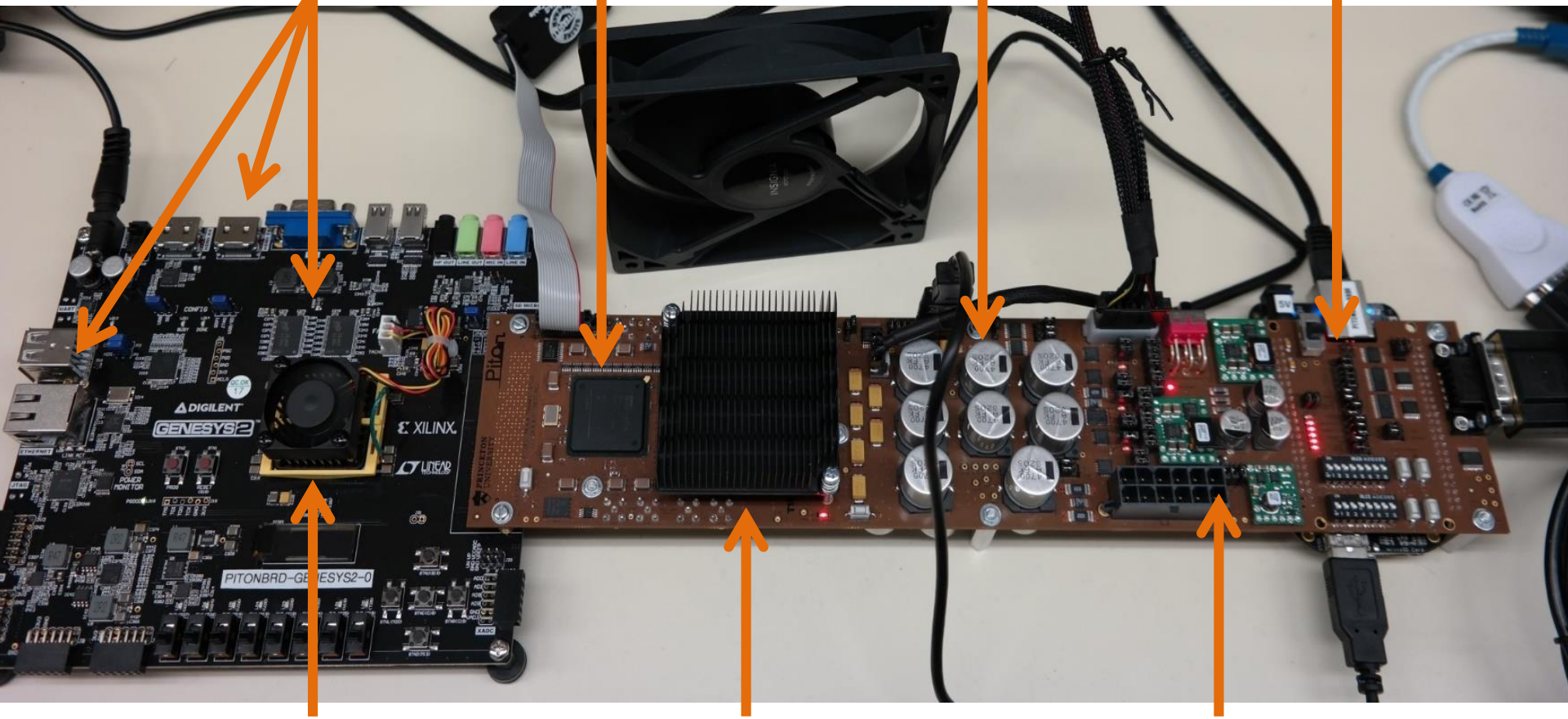


Unlidded Piton Chip



Piton Chip

Piton Test Setup



[McKeown et al, HotChips 2016] [McKeown et al, IEEE MICRO 2017] [McKeown et al, HPCA 2018]

Tetris on Debian Linux on Piton

From Michael McKeown <mmckeown@PRINCETON.EDU>
Subject **Tetris on Piton!!**
To ee-parallel@Princeton.EDU <ee-parallel@Princeton.EDU>

Reply | Reply All | Forward | Archive | Junk | Delete | More

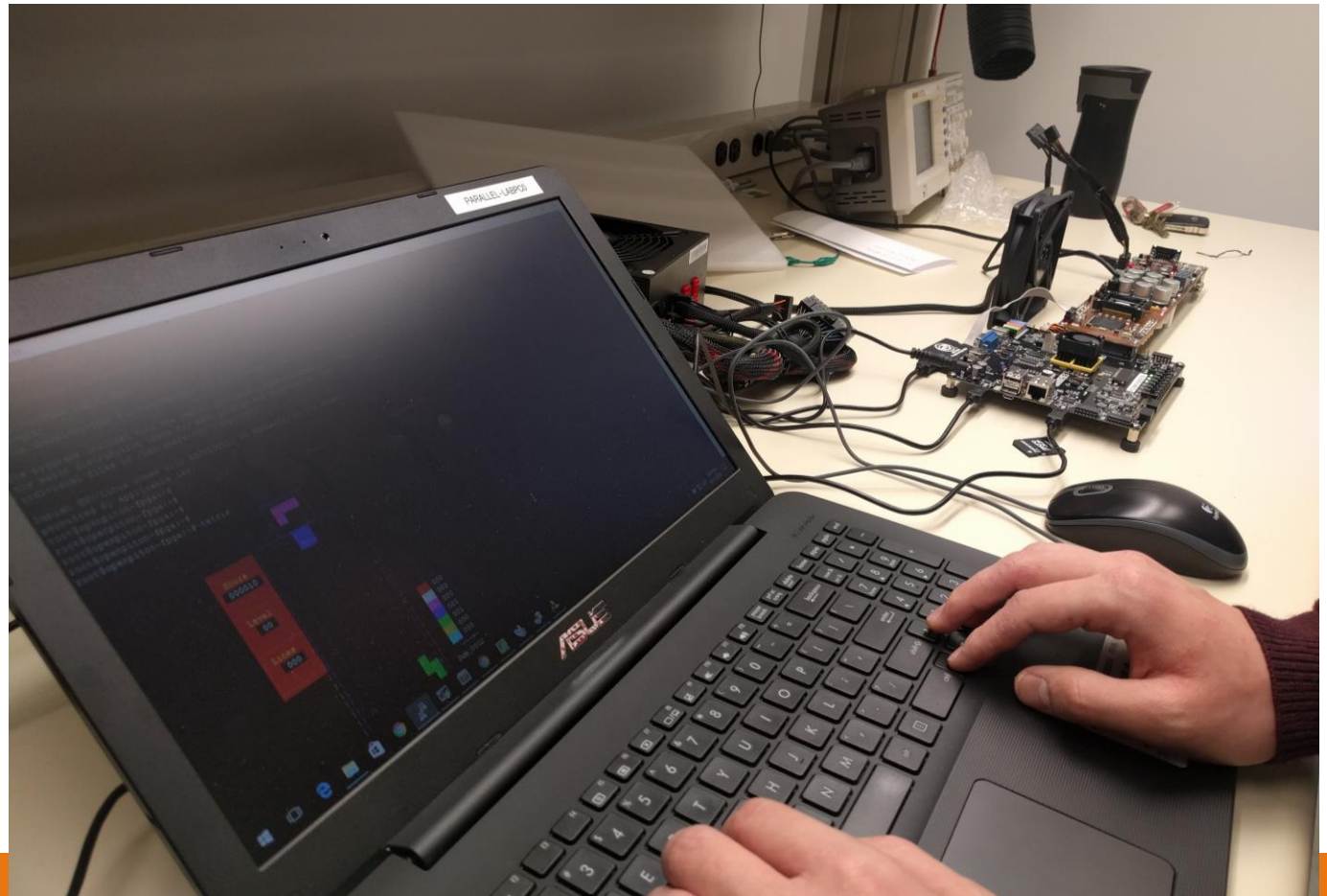
10/11/16, 5:44 PM

Piton boots Linux and we can play tetris!

Solution was to use another chip :).

Mike

IMG_20161011_174325.jpg



Tested FPGA Boards

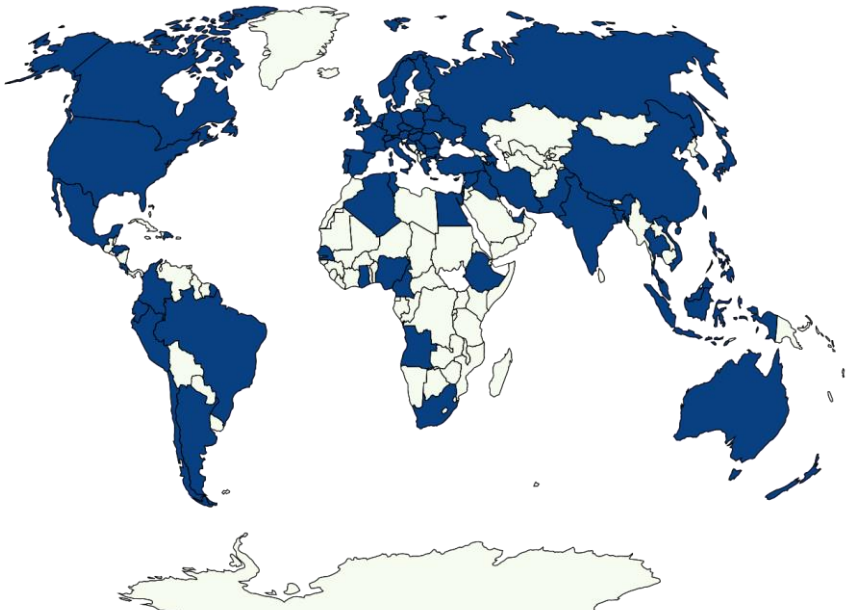
Board	Core Clock (1 core)	# of Cores	DDR Type, Size, Width	Price (academic)
Xilinx VC707 Virtex-7 XC7VX485T	60 MHz	3	DDR3, 1GB, 64 bit	$3,495
Digilent Genesys2 Kintex-7 XC7K325T	66.67 MHz	2	DDR3, 1GB, 32 bit	$1,299 ($600)
Digilent NexysVideo Artix-7 XC7A200T	30 MHz	1	DDR3, 512MB, 16 bit	$490 ($250)
Digilent Nexys 4 DDR Artix-7 XC7A100T	29MHz	1	DDR2, 128MB, 16 bit	$320 ($160)
Xilinx ZC706 Zynq-7000	66.67MHz	?	DDR3, 1GB, 64 bit	$2,495
Xilinx ML605 Virtex-6	18MHz	2	DDR3, 512MB, 64 bit	$1,995

OpenPiton Philosophy

- Focus/Value is in the Uncore
  - Not religious about ISA
  - Provide whole working system
- We are practical
  - Use Verilog
  - Industry standard tools
  - Use the best tool for job (including commercial CAD tools)
- Primarily for research, but welcome industry also
- Licensing
  - All our code, Hypervisor, are BSD-like
  - Linux, T1 core (GPL or LGPL)
- Scalability (Million Core)

OpenPiton Community

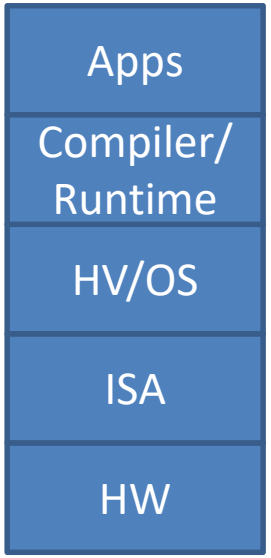
- Building a community
  - Welcome community contributions
  - Over 2000 Downloads
- Google Group



- Visit http://openpiton.org
- openpiton@princeton.edu

Doing Research with OpenPiton

- Software
  - Install on Debian, test scalability
- Operating System
  - Recompile kernel, rebuild SW, run
- Hardware/Software Co-design
  - Add new instructions, change compiler/HV/OS/SW
- Architecture
  - Change parameters, rebuild HW, run



Enabled Research

- Coherence Domain Restriction
  - Fu et al. MICRO 2015
- Execution Drafting
  - McKeown et al. MICRO 2014
- Memory Inter-arrival Time Traffic Shaper
  - Zhou et al. ISCA 2016
- Oblivious RAM
  - Fletcher et al. ASPLOS 2015
- DVFS modelling
- Multiple outside papers
- Numerous class research projects