Getting to Work with OpenPiton

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http://openpiton.org
Extension Using NoCs
NoC Connected I/O and Accelerators

10 Gigabit Ethernet

Deserializer

Serializer

DMA

Buffer

Tile

Accel

DRAM

DRAM
CHIPIID: Highest bits indicate whether the destination is on-chip or off-chip, the rest of the bits indicates the chip ID
XPOS: The position of the destination tile in the X dimension
YPOS: The position of the destination tile in the Y dimension
FBITS: The router output port to the destination
PAYLOAD LENGTH: The number of payload packets
RESERVED: Reserved Bits used by higher-level protocols.
NoC: .h files

piton/design/include/network_define.h
Defines the header flits b63-22
(all except messageid, tag, and options 1)

piton/design/include/define.vh
defines the rest

```cpp
181 //Memory requests from L2 to DRAM
182 `define MSG_TYPE_LOAD_MEM     8'd19
183 `define MSG_TYPE_STORE_MEM    8'd20
184
196 //Memory acks from memory to L2
197 `define MSG_TYPE_LOAD_MEM_ACK  8'd24
198 `define MSG_TYPE_STORE_MEM_ACK 8'd25
199 `define MSG_TYPE_NC_LOAD_MEM_ACK 8'd26
200 `define MSG_TYPE_NC_STORE_MEM_ACK 8'd27
```
Cache Coherence Protocol

Directory-based MESI coherence Protocol
- Four-hop message communication (no direct communication between private L1.5 caches)
- Uses 3 physical NoCs with point-to-point ordering to avoid deadlock
- The directory and L2 are co-located but state information are maintained separately
- Silent eviction in E and S states
- No need for acknowledgement upon write-back of dirty lines from L1.5 to L2, but writeback guard needed in some cases.
Memory Hierarchy Datapath

Private L1.5 -> Distributed shared L2 -> Off-chip Chipset

NoC1 <-> NoC1
NoC2 <-> NoC2
NoC3 <-> NoC3
NoC Messages

In order to avoid deadlock, NoC3 messages will never be blocked.