OpenPiton+Ariane: The RISC-V Hardware Research Platform

Princeton University and ETH Zürich

http://openpiton.org
http://pulp-platform.org
Extension Using P-Mesh NoCs
P-Mesh NoC Connected I/O and Accelerators
P-Mesh NoC: packet format

<table>
<thead>
<tr>
<th>Bit 63</th>
<th>Bit 50</th>
<th>Bit 49</th>
<th>Bit 42</th>
<th>Bit 41</th>
<th>Bit 34</th>
<th>Bit 33</th>
<th>Bit 30</th>
<th>Bit 29</th>
<th>Bit 22</th>
<th>Bit 21</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIPID</td>
<td>XPOS</td>
<td>YPOS</td>
<td>FBITS</td>
<td>PAYLOAD LENTH</td>
<td>RESERVED</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PAYLOAD PACKET 1

...  

PAYLOAD PACKET N

CHIPID: Highest bits indicate whether the destination is on-chip or off-chip, the rest of the bits indicates the chip ID
XPOS: The position of the destination tile in the X dimension
YPOS: The position of the destination tile in the Y dimension
FBITS: The router output port to the destination
PAYLOAD LENGTH: The number of payload packets
RESERVED: Reserved Bits used by higher-level protocols.
P-Mesh NoC: .h files

piton/design/include/network_define.h
Defines the header flits b63-22
(all except messageid, tag, and options 1)

piton/design/include/define.vh
defines the rest

//Memory requests from L2 to DRAM
```
181 //Memory requests from L2 to DRAM
182 `define MSG_TYPE_LOAD_MEM  8'd19
183 `define MSG_TYPE_STORE_MEM  8'd20
```

//Memory acks from memory to L2
```
196 //Memory acks from memory to L2
197 `define MSG_TYPE_LOAD_MEM_ACK  8'd24
198 `define MSG_TYPE_STORE_MEM_ACK  8'd25
199 `define MSG_TYPE_NC_LOAD_MEM_ACK  8'd26
200 `define MSG_TYPE_NC_STORE_MEM_ACK  8'd27
```

//Should always make #0 an error
```
144 //Requests from L15 to L2
145 // Should always make #0 an error
146 `define MSG_TYPE_RESERVED  8'd0
147 `define MSG_TYPE_LOAD_REQ  8'd31
148 `define MSG_TYPE_PREFETCH_REQ  8'd1
149 `define MSG_TYPE_STORE_REQ  8'd2
150 `define MSG_TYPE_BLK_STORE_REQ  8'd3
151 `define MSG_TYPE_BLKINIT_STORE_REQ  8'd4
152 `define MSG_TYPE_JOB_REQ  8'd5
153 `define MSG_TYPE_JOB_P1_REQ  8'd6
154 `define MSG_TYPE_JOB_P2Y_REQ  8'd7
155 `define MSG_TYPE_JOB_P2Y_REQ  8'd8
156 `define MSG_TYPE_JOB_P2N_REQ  8'd9
157 `define MSG_TYPE_JOB_P2N_REQ  8'd10
158 `define MSG_TYPE_SWAP_REQ  8'd11
159 `define MSG_TYPE_SWAP_P1_REQ  8'd12
160 `define MSG_TYPE_SWAP_P2_REQ  8'd13
161 `define MSG_TYPE_WS_REQ  8'd14
162 `define MSG_TYPE_WBGUARD_REQ  8'd15
163 `define MSG_TYPE_NC_LOAD_REQ  8'd16
164 `define MSG_TYPE_NC_STORE_REQ  8'd17
165 `define MSG_TYPE_NC_INTERRUPT_FWD  8'd18
```
P-Mesh Cache Coherence Protocol

Directory-based MESI coherence Protocol
- Four-hop message communication (no direct communication between private L1.5 caches)
- Uses 3 physical NoCs with point-to-point ordering to avoid deadlock
- The directory and L2 are co-located but state information are maintained separately
- Silent eviction in E and S states
- No need for acknowledgement upon write-back of dirty lines from L1.5 to L2, but writeback guard needed in some cases.
Support for RISC-V Atomic Operations

Arithmetic Operations
- L2 cache invalidates all sharers
- Perform the operation with an ALU in the L2 cache

Load-Reserve and Store-Conditional (LR/SC)
- L1.5 cache maintains the flag for LR/SC
- Upon LR, the cache line's MESI state is set to M (MODIFIED) and the LR/SC flag is set to high
- Operations that change the line's MESI state will clear the LR/SC flag
Memory Hierarchy Datapath

Private L1.5 → Distributed shared L2 → Off-chip Chipset

NoC1, NoC2, NoC3
NoC Messages

In order to avoid deadlock, NoC3 messages will never be blocked.

Diagram:
- L1.5
- L2
- L1.5/Memory

Messages:
- Load
- Store
- Ifill
- ... (other messages)
- NoC1
- NoC2
- NoC3
- DG ack
- Inv ack
- Mem Reply
- Load Ack
- Store Ack
- ... (other messages)