Organic-Flow: An Open-Source Organic Standard Cell Library and Process Development Kit

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***Abstract*—Organic thin-film transistors (OTFTs) are drawing increasing attention due to their unique advantages of mechanical flexibility, low-cost fabrication, and biodegradability, enabling diverse applications that were not achievable using traditional inorganic transistors. With a growing number of complex applications being proposed, the need for expediting the design process and ensuring the yield of large-scale designs with organic technology increases. A complete digital standard cell library plays a crucial role in integrating the emerging organic technology into existing computer-aided-design (CAD) flows.**

In this paper, we present the design, fabrication, and characterization of a standard cell library based on bottom gate, top contact pentacene OTFTs. We also propose a commercial tool compatible, RTL-to-GDS flow along with a new organic process design kit (PDK) developed based on our process. To the best of our knowledge, this is the first open-source organic standard cell library, enabling the community to explore this emerging technology.

I. Introduction

While the development of computing technology has made our lives easier, this convenience has come at the cost of pollution to our environment caused by large quantities of electronic waste (e-waste). Furthermore, the global production of e-waste is expected to accelerate in the near future due to billions of connected devices being deployed as part of the Internet of Things (IoT). Unlike most other waste, electronic devices are acutely difficult to recycle due to their highly heterogeneous nature. There is thus an urgent need to design sustainable electronics that ideally have no harmful impact on the environment from both an operational energy, materials consumed, and end-of-life perspective.

Biodegradable organic electronics that are environmentally safe, low-cost, large-volume, and disposable have emerged as a desirable and, in principle, straightforward solution to this urgent e-waste pollution problem [1]. Biodegradable electronics exhibit transient behavior, being capable of serving their function over prescribed time frames before physically disappearing, being metabolized by microorganisms into non-harmful constituents.

In addition to alleviating the growing problem of e-waste, the properties of biodegradability also enable electronics to be used across large areas, including environmental sensors, packaging, and medical implants, which were inaccessible for traditional inorganic compounds. With impressive improvements in materials and electrical performance over the past three decades, organic thin-film transistors (OTFTs) have proven to be competitive for existing and novel applications [2].

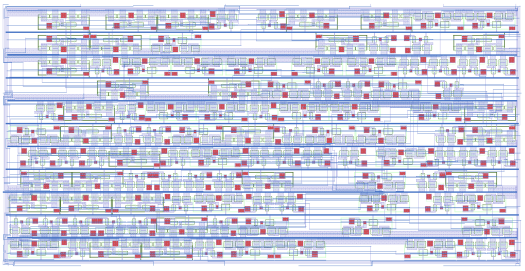

Fig. 1: Layout image of a placed and routed organic thin-film transistor-based 8-bit adder designed with Organic-Flow

However, moving to organic semiconductors poses many new challenges, including approximately 1,000 times lower electron mobility when compared to silicon, larger minimum feature size limited by material degradation and dissolution during photolithographic patterning, less uniformity and stability causing a significant variation in device current and threshold voltage, and the need to use unipolar design since high-performance organic semiconductors are usually p-type and organic n-type materials tend to be less stable.

With a growing number of complex applications being proposed, **the need for expediting the design process of large-scale design with organic technology rises and a digital standard cell library plays a crucial role** in integrating the emerging organic technology into existing computer-aided-design (CAD) flows. In this work, we design and characterize a standard cell library comprised of basic combinational and sequential building blocks based on organic thin-film transistors. We implement an industrial tool compatible RTL-to-GDS flow with an organic process design kit (PDK) based on our fabrication process technology. Using this flow, a fully placed and routed 8-bit adder generated from Verilog RTL is shown in Fig. 1. The Organic-Flow will enable other researchers to analyze the organic circuit/architecture performance, study the implications of organic semiconductors, and build complex designs. The Organic-Flow is available for download from `http://parallel.princeton.edu/organicflow`.

Our work makes the following contributions:

- Creation and characterization of an organic semiconductor standard cell library using **experimentally validated** OTFT device models.

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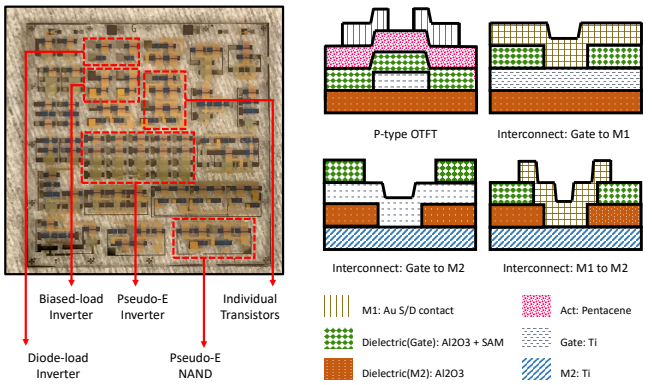
- Demonstration of a complete RTL-to-GDS flow including synthesis, placement, and routing of complex digital designs in organic semiconductors.
- Release of the first open-source organic standard cell library and the compatible organic process design kit (PDK) to enable other researchers to build upon this work.



(a) (b)

Fig. 2: (a) Photograph of a fabricated 3 × 3 cm OTFT circuit integrated sample (b) The cross-sectional views of the OTFT and interconnects between each metal layer

II. Organic Technology

There has been significant progress in OTFT processes in recent decades, from materials to systems. As a result, OTFTs have transitioned from lab curiosity to a potentially viable commercial product. In this section, we discuss the applications, challenges, and fabrication process of OTFTs that we developed in our lab.

A. Applications

As the popularity of IoT continues to rise due to emerging applications and falling device costs, billions or even trillions of Internet-connected electronic devices are likely to be distributed throughout our world. Building all of these emerging electronic devices using traditional silicon platforms means considerable e-waste that is difficult to recycle when these devices reach the end of life. Also, a massive amount of energy is consumed during the fabrication process of high-quality inorganic semiconductors and other nanomaterials [1]. The increased embodied energy from electronic products also hinders sustainability.

Organic semiconductors serve as a qualitative game changer and show the potential of solving this problem. Biodegradable electronics can not only decompose in a reasonable period as determined by the proposed application, but also require less energy during the manufacturing process. The rapid development of biodegradable electronics motivates a series of new potential applications such as environmental sensors and medical electronics for drug release. The need to recycle these sensors for applications requiring embedded computing with modest computing requirements can therefore be removed. In addition to biodegradability, the potential for low-cost OTFT systems also makes them ideal for inexpensive, flexible, large-area, and disposable applications. Organic RFID tags are being aggressively used for applications like supply chain management since they are inexpensive enough to be widely deployed. In addition, organic sensor arrays are attractive due to the potential compatibility with highly selective biological recognition elements like enzymes.

One aspect barring biodegradable electronics from the commercialization or being used in computing and complete sensing devices is the lack of a fully automated design flow integrated with electronic design automation (EDA) tools, an aspect we develop here. This development will play a crucial role in expediting the design process and exploring the application possibilities for organic semiconductors.

B. Challenges

Circuits based on OTFTs face several challenges. First, the typical carrier mobility of organic semiconductor is around 1 $cm^2V^{-1}s^{-1}$, three orders of magnitude lower than crystalline silicon. The low mobility fundamentally limits the operating frequency of the OTFT circuits. Second, high-resolution patterning of organic semiconductors is difficult. Photolithography suffers from material degradation and/or dissolution in photoresist subtractive processes. Shadow mask patterning, commonly used for organic material patterning, which uses metal screens with patterned holes in front of the substrate, suffers from limited resolution and alignment accuracy. Thirdly, high-performance organic semiconductors are usually p-type. The complementary application of OTFT circuits usually requires incorporating less-reliable n-type organic semiconductors or hybrid systems involving n-type metal oxides, resulting in increased fabrication complexity, device area, and/or instability. Finally, OTFT circuits suffer from non-uniformity and ambient instability.

C. Fabrication

The transistors we fabricate and characterize are based on a bottom gate, top contact structure. Pentacene is chosen as the p-type material, mainly due to its status as an archetypal p-type organic semiconductor that has been highly studied. The transistor and circuit layouts are illustrated in Figure 2. Our circuits use a 3 × 3 cm Eagle XG glass substrate. The gate electrode is 50 nm thick Titanium (Ti) sputtered at 2 Å/s. Our gate dielectric is 50 nm of Al_2O_3 and is grown by atomic layer deposition (ALD). The Ti gate and the via hole through the dielectric layer are patterned through wet etching. The sample is treated with octadecyl trichlorosilane (OTS) self-assembled monolayer (SAM) for better control of morphology and carrier injection of the pentacene layer. Finally, 50 nm of pentacene and 50 nm of gold (Au) source and drain contacts are thermally evaporated through a thin metal shadow mask.

III. Organic Standard Cell Library

Currently, implemented OTFT circuits are still typically device-based, and designers end up hand-drawing large final

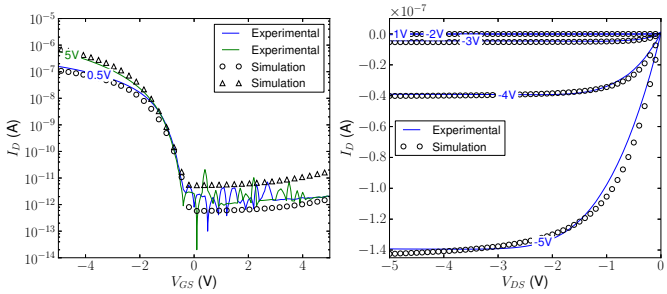
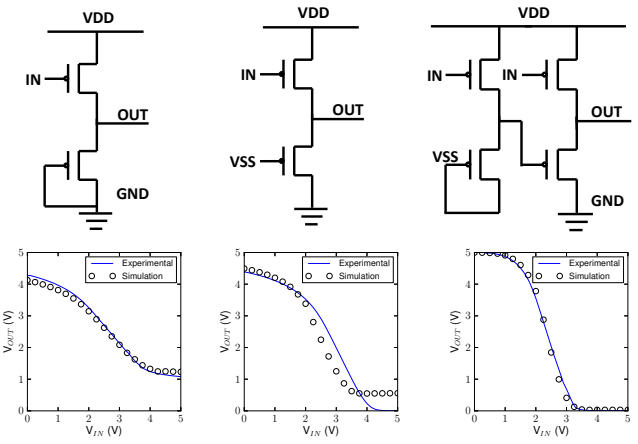


Fig. 3: Comparison of measured and modeled static output and transfer characteristics of an OTFT



(a) diode-load (b) biased-load (c) pseudo-E design

Fig. 4: Schematics and experimental and simulation voltage transfer characteristics of inverters based on (a) diode-load, (b) biased-load, or (c) pseudo-E design.

circuit layouts, which is not a scalable approach to designing complex systems. To facilitate the design of organic circuits and ensure good yield for complex circuit systems, the community needs to establish consistent design methodology and introduce rigorous verification. In this section, we present the development of an organic standard cell library based on experimentally fabricated and measured OTFTs.

A. Transistor Characterization and Device Curve Modeling

First, we build a detailed OTFT model through careful measurement of our fabricated OTFTs. We developed this process, designed the circuits, and tested them all at our institution. The current-voltage (I-V) characteristics of OTFT with a channel length 80 μm and width 1000 μm are measured with a probe station in a nitrogen-filled glovebox, using the HP4155A parameter analyzer. As shown in Fig. 3, transistors show good on-to-off current ratio and close-to-zero threshold voltage.

A compact SPICE device model is essential to design and simulate the behavior of complex integrated circuits. However, the basic MOSFET model based on silicon is insufficient to characterize OTFTs due to the lack of compatibility with the multiplicity of processes and structures in organic technologies. The RPI amorphous silicon TFT model [3] is adapted

TABLE I: Extracted inverter parameters

Inverter type	Diode-Load	Biased-Load	Pseudo-E
V_M (V)	2.5	2.6	2.4
V_{SS} (V)	/	-2	-6
Gain	1.1	2.0	3.1
NM_H (V)	0.05	0.4	1.3
NM_L (V)	0.1	0.6	1.3
Power (μW)	1.5	3.0	1.7

here to model the OTFT behavior. Though originally developed for amorphous Si (a-Si) rather than organic semiconductors, the model is designed for a 3-terminal accumulation mode transistor, with adequate parameters to describe carrier mobility, the sub-V_T region, and leakage current characteristics. To adjust the models, we first consider static behavior. Model parameter extraction was conducted through fitting transfer and output curves between the models and fabricated devices. Fig. 3 plots the data simulated with the SPICE device model against the experimental data measured, which is close to the predicted value. This model is used to predict the behavior of the organic logic gates of the standard cell library.

B. Design of Standard Cells

The proposed standard cell library consists of 6 basic logic cells which can be used to cover all required logic functions. In this work, we use p-type only transistor design since organic p-type TFTs offer better performance and stability over n-type TFTs. In the following section, we use an inverter as an example to illustrate the design flow of a standard cell and discuss the tradeoffs between different design styles.

1) Design of an Inverter: Fig. 4 shows the schematics and measured versus modeled static voltage transfer characteristics (VTC) based on three types of logic designs: diode-load, biased-load, and pseudo-E [4]. The diode-load and biased-load inverters have simpler structures but deliver poor performance. In contrast, the additional level shifter stage added in the pseudo-E inverter allows the bias voltage of the load transistor to depend on the input voltage and provides rail-to-rail output voltage swing. As summarized in Table I, the performance of the pseudo-E inverter increases dramatically with the negatively biased terminal of the level shifter. Though requiring twice the transistor count, the pseudo-E type inverter has a more controllable and desirable performance and is therefore selected as the design style for the whole library. As shown in Fig. 4, the SPICE model built in Sec. III-A fits the transfer characteristics well, especially for the pseudo-E type inverter.

2) Other Standard Cells: We repeat the above analysis for NAND and NOR gates, using only the pseudo-E design as only the pseudo-E design achieves full voltage swing with short gate delay. The functionality is verified through measuring the transient behavior of fabricated gates The heights of the gates are fixed to facilitate the placement process by allowing better cell alignment and power rail sharing.

To speed up fabricated circuits and provide the synthesis tool more choice of gates, we also design three-input NAND and NOR gates, using similar structures to the two input cases.

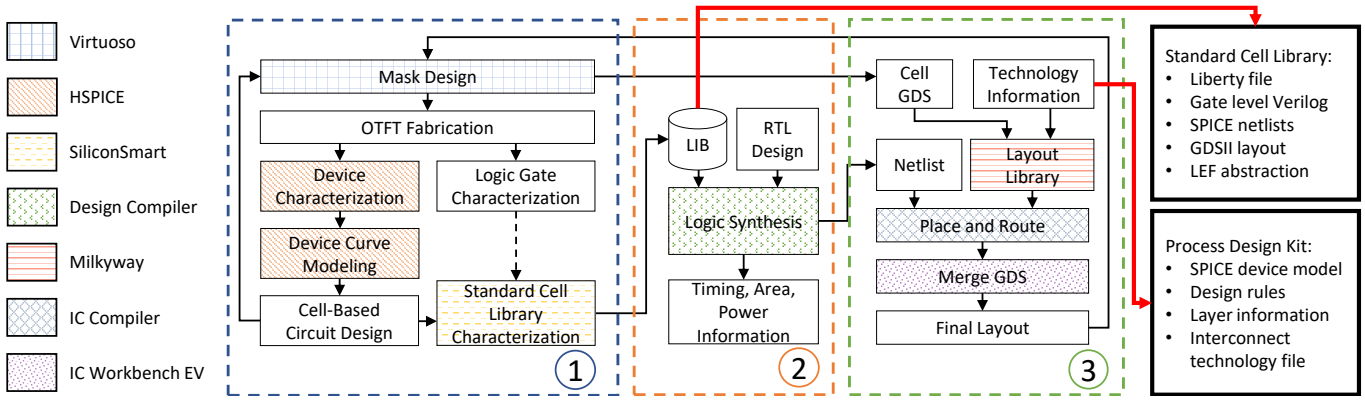


Fig. 5: Organic design flow

In addition to the universal logic gate family, a register is also necessary for sequential logic. We implement a D-flip-flop with preset and clear.

The fine-tuning of circuit sizing is important for creating a good logic gate. Since adjusting the parameters and running simulations manually is time-consuming, we automate the design space exploration by defining a utility function to evaluate the quality and efficiency of the gates built with different parameter sets. Then we select the best parameter sets for each transistor size. The switching threshold, noise margin, voltage swing, gate delay, and area are all taken into consideration when choosing the transistor size.

C. Cell Characterization

The organic standard cell library is characterized by the nonlinear delay model (NLDM), which is a simple and fast voltage-based model. The NLDM models gate delay and output slew as a nonlinear function of input transition time (i.e. slew) of the cell and the output effective capacitive load. The timing and power information derived from the set of SPICE characterizations is then formatted into look-up tables (LUT). We use Synopsys SiliconSmart as the library characterizer to generate a library in Liberty format from a set of process models, cell functional descriptions, and associated SPICE netlists. The generated library (.lib) is validated for cell sensitivity, minimum load, data range, and power pin consistency. It can be then used for timing, power, and area analysis with compatible tools.

IV. Organic RTL-to-GDS Design Flow

As indicated by Guo et al. in [5], a full EDA toolchain for OTFT-based systems has not yet been developed. This has become a problem as OTFT designs mature and researchers and industry begin to design more complex systems and move to mass production. Fortunately, sharing some commonality with silicon transistors, OTFTs are able to adapt similar techniques widely used in the conventional silicon industry. To use the existing technology-dependent EDA tools, a PDK needs to be built from scratch since the major characteristics and materials for organic technology are totally different. In this section, we present the development of the world's first open-source full RTL-to-GDS flow using the standard cell library we characterize and the PDK files developed for using physical implementation tools.

A. Organic Design Flow

Fig. 5 shows the library characterization and RTL-to-GDS flow using the proposed organic library. The tools we used for each step are listed on the left. Users will be able to download our standard cell library, write their own design in RTL, and run the full tool flow to estimate the timing and power and obtain the layout in GDSII format for fabrication.

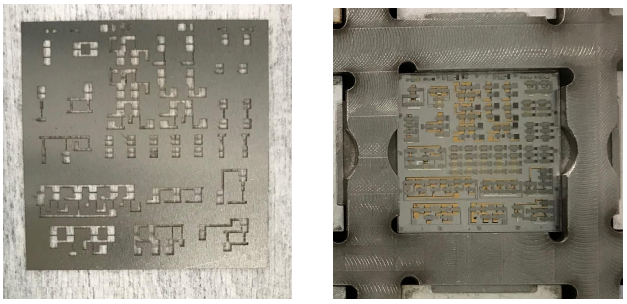
Part ① illustrates the steps of cross-validating our cell library. The output of the timing and power characterization, which is a Liberty timing file (.lib), is passed to the logic synthesis tool. Part ② shows the synthesis flow. The RTL of the desired design, along with design constraints are first passed to the logic synthesis tool, which synthesizes a gate-level netlist from the behavioral RTL and generates the timing, power, and area reports for the synthesized design. The minimum clock period and area can then be estimated.

As shown in part ③, the resulting gate-level netlist, along with the constraints, are passed to the physical implementation tool to perform placement and routing (PnR). To create a layout library in the EDA database format used by the physical design tool, we first extract Library Exchange Format (LEF), a specification for representing the abstraction of physical layout, from the mask used in fabrication and check the geometry and blockage for every cell. We then define the organic technology files with mask layer information, appropriate sizing, and design rules based on our real device fabrication experiences. Supplying the layout library in conjunction with the gate-level netlist to the PnR tool, the users can get the placed and routed designs in GDSII format and more accurate timing, area, and power reports as the output. Since the abstraction of pins in cells is used for placement, the final step is merging the full layout of the standard cells back and obtaining the final layout.

The **release** of this first open-source organic standard cell library, including circuit design, timing characterization, and layout information of each cell, OTFT device model, and the PDK containing technology-related files in tool-compatible format shortens design time.

TABLE II: Layer map

Layer Name	Description	Mask Name	Minimum Dimension(μm)	
			Width	Spacing
Gate	Metal gate conductor made of Ti	metal2	20	10
Act	Active area (pantacene)	active	100	50
M1	First-level metal line made of Au	metal3	100	50
V1	Via for connecting Gate and M1	via2	20	10
M2	Second-level metal line made of Ti	metal1	20	10
V2	Via for connecting Gate and M2	via1	20	10



(a) (b)

Fig. 6: (a) The shadow mask of the source/drain electrodes (M1) (b) The shadow mask patterning process, the sample (top) and mask (bottom) are confined in a grid

B. Physical Design Flow

For the standard cell based physical design flow to work correctly, we need to provide technology-dependent information, like design rules, layer mapping, and parasitic models, in addition to the timing library file. All these files are included in the release PDK. Table II summarizes the 6 different mask layers in the presented OTFT technology and the basic design rules of each layer. The design rules are defined based on the fabrication experiences and alignment restrictions of our standard OTFT fabrication flow (developed by our group) and are due to technology characteristics.

As mentioned in Sec. II, our devices are fabricated based on a bottom-gate, top-contact structure, which is generally incompatible with conventional photolithography for the deposition of source/drain electrodes on top of organic semiconductors due to organic semiconductors' intolerance to solvents. Thus we use shadow mask patterning for the Active and M1 layers as shown in Fig. 6. Shadow mask patterning is simpler than photolithographic patterning and can effectively protect the pentacene active layer from damage caused by subsequent solution processing, but also has notable resolution limitations on alignment due to the lack of position control during the patterning process. The minimum width and spacing thus increase, as shown in Table II. To compensate for the possible alignment error, we make the design rules more conservative to increase the yield, which has been a critical issue for scaling-up functioning circuit size. Tighter tolerances on minimum width and spacing are achievable through better alignment technology and developing patterning methods.

Another difference compared to silicon CMOS gate designs lies in power rail sharing. Since pseudo-CMOS style logic gates require an additional bias voltage rail other than normal VDD and GND, it is impossible to share all the power rails between neighboring rows by vertically flipping the same-height standard cells as in traditional silicon technology. In our standard cell library, VDD and GND are shared while the third power rail, VSS, is designed to be at the same height for all the cells in order to reduce the extra routing. More design rules, such as the spacing between different metal and via layers, can be found in the released PDK.

The choices of materials, device structures, fabrication techniques, and alignment constraints differ from one OTFT process to another. However, the released technology files can serve as a starting point that has been shown to be fabricatable, where device researchers can tune the parameters to accommodate their needs and use the provided scripts to generate the design of a more complex circuit.

TABLE III: Summary of several synthesized designs

Design	Area (mm^2)	Cell Count	Frequency (Hz)
Parity Checker	340	32	1923
8-bit Adder	884	82	1471
openMSP 430	76332	7477	185.2

C. Challenges

Developing a robust and high-performance digital library for a new semiconductor technology is a challenging task. For organic technology, one of the main challenges is providing reasonable routability given limited metal layers other than the gate metal. Fig. 2b shows the cross-sectional views of three metal layers we have and how they are connected. Notably, the metal2 layer (M2) is located at the bottom of the gate instead of on the top of M1, and contacts/vias are not needed between source/drain and M1. Since only standard mask names are recognized, we need to remap the layers in organic technology to existing infrastructure for the conventional silicon process as shown in Table II to utilize the power of existing tools.

Defining the design rules is also difficult. There is a trade-off between yield (affected by the ease of fabrication) and the performance improvement obtained from aggressively optimized sizing and spacing. For example, the minimum width of metal1 listed in Table II is made wider to account for the potential alignment error. Organic technology is still being actively developed, and many technical details in the toolchain remain to be further optimized. The release of this paper, the open-source standard cell library and PDK will benefit both system designers and device researchers by revealing the semiconductor characteristics and shortening the design cycle.

D. Results

To show how to integrate the standard cell library designed in Sec. III into the back-end flow, we synthesize some small designs and a simple processor core with the timing library based on the organic technology and present the GDSII layouts generated with the help of CAD tool flow. We choose a parity checker, an eight-bit adder, and a microcontroller core (openMSP430) as a target design to verify the organic flow. Table III summarizes the area, cell count, and frequency of these three designs synthesized with our cell library. The maximum

TABLE IV: Properties and scopes of Related Work

Work	Process	Cell Library	Timing Library	Full PDK	Physical Design Flow	Open-Source
[6], [7], [8]	OTFT	✓	✗	✗	✗	✗
[9]	OTFT	✓	✓	✗	✗	✗
[10]	OTFT	✗	✗	✓	✓	✗
[11]	OTFT	✗	✗	✓	✓	✓
[12]	CNT-TFT	✓	✗	✓	✗	✗
[13]	OTFT	✓	✗	✓	✗	✗
Organic-Flow	OTFT	✓	✓	✓	✓	✓

frequency is estimated by running through multiple passes of synthesis and the reported critical path will enable the analysis of the timing and further optimization of the design considering the underlying semiconductor characteristics.

With the synthesized netlist, we run the place and route flow for both the parity checker and the adder. The core utilization rate is roughly 70% for both of the designs. Optimization of the spacing rules, the number of routing tracks allowed, and using more aggressive mask design, would further increase the density of the transistors. We believe that the auto placement and routing flow will significantly shorten the design cycle while improving the quality of the layout.

V. Related Work

As listed in Table IV, several standard cell libraries have been implemented for OTFTs previously, either being used to cross-validate the simulation and real measurements [6], [7], [8] or evaluate different architectural designs [9]. Unfortunately, none of these standard cell libraries are released to the public. Our work focuses on building the full back-end flow for OTFT technology and releasing the library along with the compatible process design kit to share the knowledge and enable more research in this field.

The resources of open-source PDKs for organic technology are very limited [10], [11], [12]. Due to the process differences, we develop a new PDK with our own design rules and provide files needed for physical implementation flow, circuit layout drawing, and validation. In addition, this work proposes the design and the release of the cell-based place and route flow, which can further scale-up and speed-up the circuit design.

Llamas et al. build a top-down flow for application-specific printed electronic circuits based on corbino OTFTs [13], which adopts hand-made placement and routing instead of automated generation like our work. As summarized in Table IV, our work (Organic-Flow) is the first open-source standard cell library designed for OTFT with compatible PDK and full physical implementation flow support.

VI. Conclusion

We have constructed Organic-Flow, a standard cell library for organic thin-film transistors along with a compatible process design kit to support complete RTL-to-GDS flow. The advantages, disadvantages, and design trade-offs between different logic gate design styles have been analyzed. The cell library is extensible for other types of organic devices. The fabrication-validated timing library enables system and circuit designers to explore design choices affected by the underlying semiconductor characteristics, and the back-end flow can expedite the large-scale layout mask design process. The release of Organic-Flow, the first open-source organic standard cell library, PDK, and a seamless design automation flow is a good start to removing barriers of entry to using organic semiconductors by system designers. This work can enable the community to work on common issues, encouraging greater technology dissemination and enable research opportunities.

VII. Acknowledgement

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