This problem set is **ungraded and not collected**. Please stop by office hours if you have questions.

Problem #1: Compute the Clocks Per Instruction (CPI) of a machine which has an average CPI for ALU operations of 1.1, a CPI for branches/jumps of 3.0, and a hit rate of 60% in the cache. A hit in the cache takes 1 cycle pipelined and a cache miss takes 120 cycles. Assume 22% of instructions are loads, 12% are stores, 20% are branches/jumps and the balance are ALU operations.

Problem #2: You are a processor designer and have to make a decision between building a processor which executes at 1GHz and has an average CPI 1.2 and a processor which executes at 2GHz, but has a CPI of 2. Which is better to build and why?

Problem #3: Page C-82 in H&P5, Problem C.1 a,b,c,d,e,f,g

Problem #4: Page B-60 in H&P5, Problem B.2 a,b

Problem #5: Draw a circuit diagram for a 2-way set associative cache that can be indexed by bytes which has 8 blocks with a block size of 8-bytes. Show the tag-match logic and the output byte-select mux. Also, assume that it is a 32-bit machine and show the number of bits of the address which goes to each multiplexer and tag-comparator.

Problem #6: For the following code snippet, identify all of the RAW, WAW, and WAR hazards. Provide a list for each hazard. Hint, remember that you have to check more than neighbor instructions.

```
ADD R1, R2, R3
SUB R3, R4, R6
MUL R5, R4, R7
ADDIU R5, R5, 1
SUB R6, R3, R9
ANDI R2, R1, R9
```

Problem #7: Page C-85 in H&P5, Problem C.6 a,b,c,d,e

Problem #8: Using graph B.9 on page H&P5 B-25 and table B.8 on page B-24. Which has a lower miss rate, a 256KB direct mapped cache or a 64-KB 8-way cache? Which of the three C’s drives the previous result?
Problem #9: Draw the pipeline diagram of the following code executing on the shown in-order two-way superscalar processor. Assume that branches execute in pipeline A, loads/stores in pipeline B. Assume full bypassing when possible and no alignment problems.

```
ADD R5, R6, R7
SUB R6, R7, R8
LW  R10, R6(0)
ADDIU R12, R13, 1
LW  R15, R6(4)
LW  R15, R15(4)
ADD R6, R9, R10
ADDIU R8, R10, R11
```

Problem #10: Given that you have an architecture which has the following pipeline stages:
F D I X0 X1 W
and that register fetch happens in the I stage of the pipeline and branch resolution happens in X1, how many dead instructions are need to be killed when a branch miss-predict is taken? Now assume that the pipeline is a three-wide superscalar, how many instructions need to be killed on a branch miss-predict? (Assume that the branch is the first instruction executing after a jump.)

Problem #11: A processor is executing code and executes a divide instruction which divides by zero.
(a) Describe in the MIPS instruction set what state needs to be saved by the hardware interrupt mechanism.
(b) Assume that the interrupt handler reads registers R5, R6, R7 and writes registers R5, R8, R10, what registers does the interrupt handler need to save.
(c) What state does the ERET instruction change?
Problem #12: An instruction takes the following synchronous exceptions: Instruction Address Exception and ALU Overflow. What should the interrupt cause be loaded with? What if that same instruction has an external interrupt pending? Explain why?

Problem #13: Assume that you have the IO2I pipeline from lecture. It can issue one instruction per cycle and can commit one instruction per cycle. Draw the pipeline diagram of the following code sequence executing.
MUL R6, R7, R8
ADD R9, R10, R11
ADD R11, R12, R13
ADD R13, R14, R15
ADD R19, R13, R10
LW R2, R3
ADD R12, R16, R19
LW R5, R2
ADD R15, R20, R21

Problem #14: Assume architecture I2OI from lecture.
Draw the state of the scoreboard when instruction 3 is in the I stage of the pipeline.
0: MUL R6, R7, R8
1: ADD R9, R6, R11
2: MUL R7, R1, R2
3: LW R10, R12